



1/4

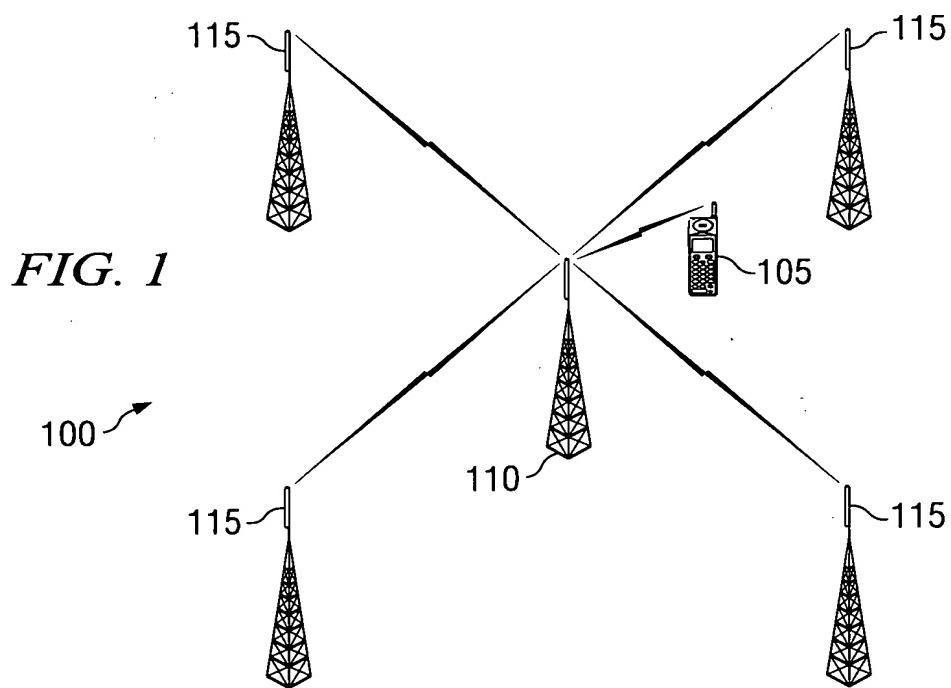
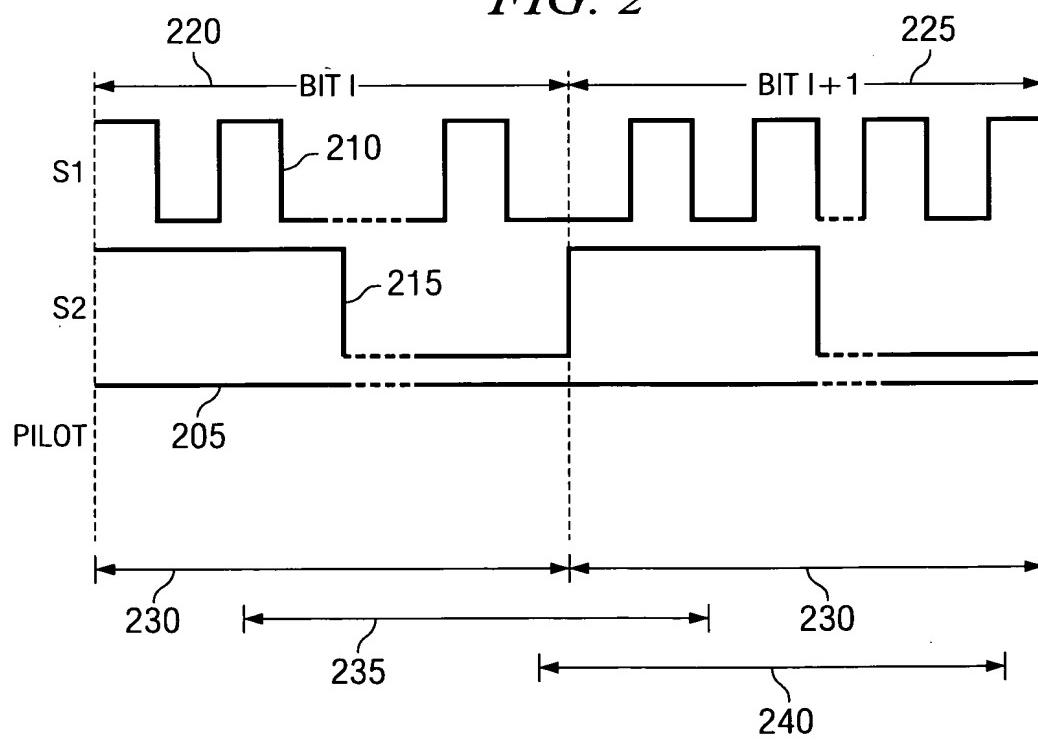
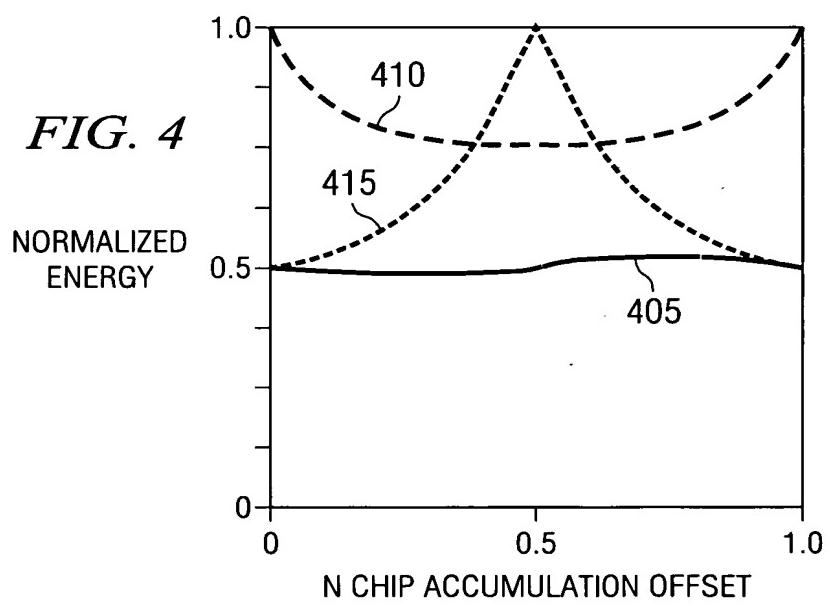
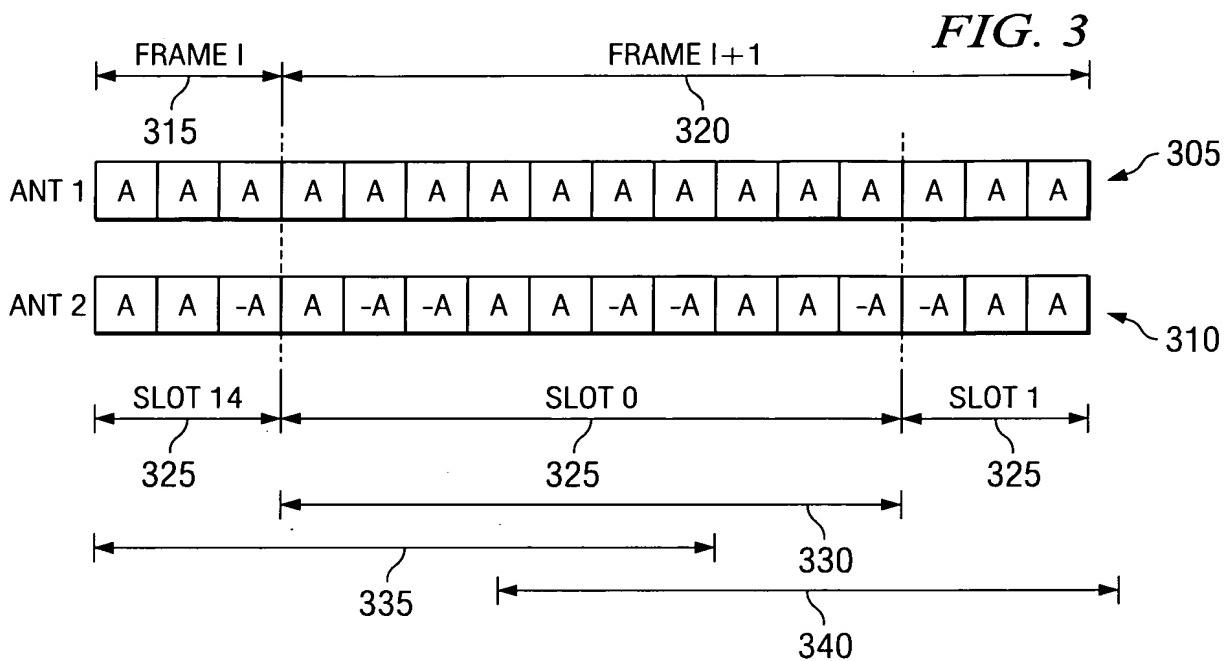


FIG. 1

FIG. 2



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*FIG. 5
(PRIOR ART)*

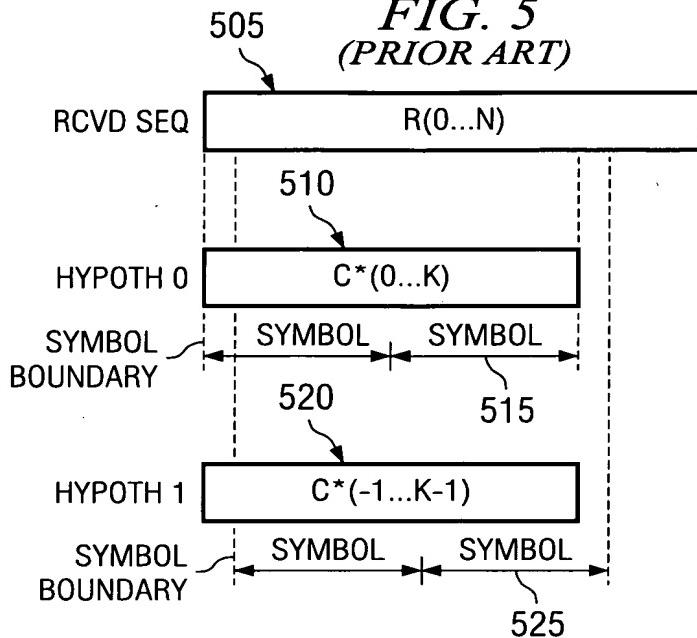


FIG. 9

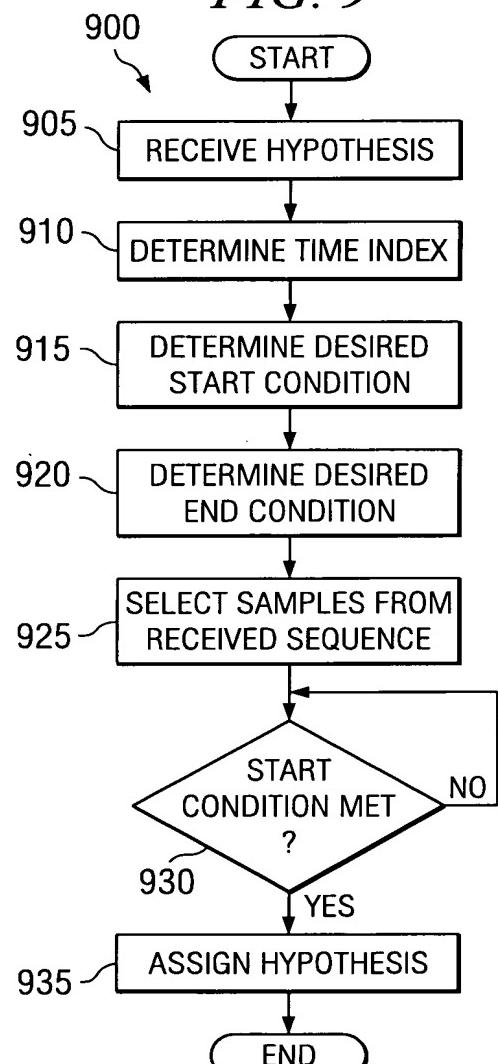


FIG. 6

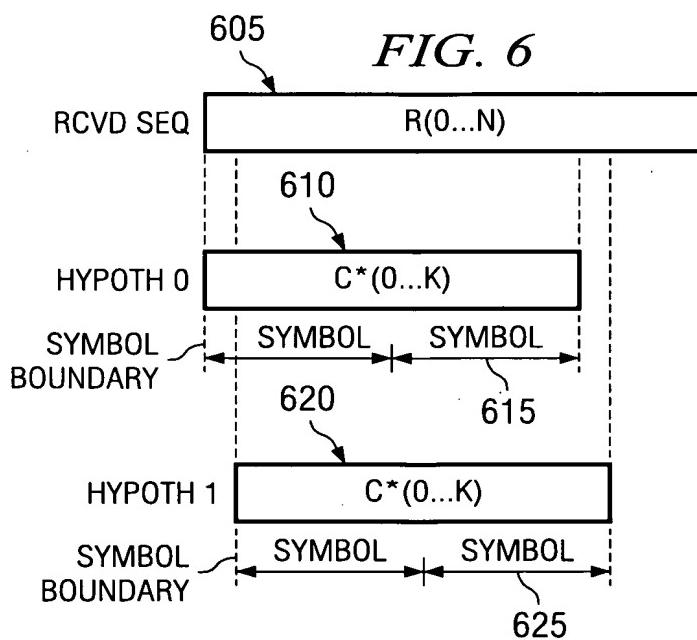


FIG. 7

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graph TD
    H[HYPOTH MEMORY] --> SC[SEARCH CONTROL]
    SC --> CAP[CAPTURE TIME]
    CAP --> SB[SAMPLE BUFFER]
    SB --> DESC[DESCRAMBLER]
    DESC --> COA[COHERENT/NON-COHERENT ACCUMULATORS]
    COA --> RP[RESULT PROCESSOR]
    RP --> TO[TO MEMORY]
    SG[SEQUENCE GENERATOR] --> SC
    SG --> CAP
    CAP --> TBC[TIME BASE CONTROLLER]
    TBC --> RCI[RADIO CONTROLLER INTERFACE]
    TBC --> CAP
    RCI --> CAP
    TBC --> CAP
    TBC --> SC
    TBC --> SG
    CAP --> SC
    CAP --> SG
    SC --> 700[700]
    SG --> 705[705]
    COA --> 711[711]
    DESC --> 713[713]
    RP --> 717[717]
    TO --> 705[705]
  
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